Low Capacitance ESD Protection Array

Features

Meet IEC61000-4-2 (ESD)±15kV (air), ±8kV (contact)

Meet IEC61000-4-4 (EFT) rating. 40A (5/50ns)

Meet IEC61000-4-5 (Lightning) rating. 12A (8/20μs)

Protects two I/O lines

Working Voltage : 5V,

Ultra-Low capacitance (around 1pF)

Pb free version, RoHS compliant, and Halogen free

Mechanical Data

Case : SOT-523 small outline plastic package

Terminal: Matte tin plated., solderable per MIL-STD-202, Method 208

Molding Compound Flammability Rating : UL 94V-O

High temperature soldering guaranteed：260^{O}C/10s

Weight : 3mg (approximately)

Applications

Cell Phone Handsets and Accessories

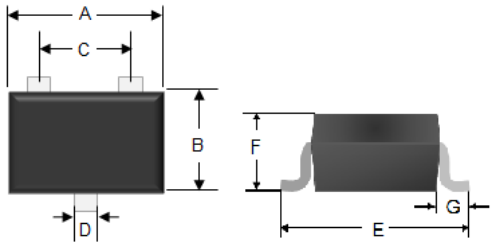
Notebooks, Desktops, and Servers

Keypads, Side Keys, USB 2.0, LCD Displays

Portable Instrumentation

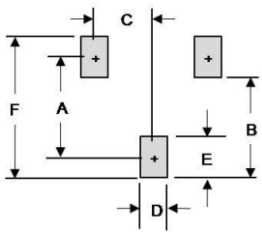
Outline Drawing

SOT-523



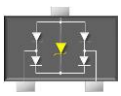
Dimension	Unit (mm)		Unit (inch)	
	Min	Max	Min	Max
A	1.50	1.70	0.059	0.067
B	0.75	0.85	0.030	0.033
C	0.90	1.10	0.035	0.043
D	0.15	0.32	0.006	0.013
E	1.45	1.75	0.057	0.069
F	0.70	0.90	0.028	0.035
G	0.56 Ref		0.022 Ref	

Suggested Pad Layout



Dim	A	B	C	D	E	F
Inch	0.055	0.055	0.020	0.016	0.031	0.087
mm	1.40	1.40	0.50	0.40	0.80	2.20

Ordering Information

Package	Part No.	Packing	Marking	Configuration
SOT-523	RESDH35V0J	3K/7" Reel	P5	

Maximum Ratings and Electrical Characteristics

(Rating at 25^{O}C ambient temperature unless otherwise specified)

Maximum Ratings

Type Number	Symbol	Value	Unit
Peak Pulse Power (tp=8/20μs waveform)	P_{PP}	100	W
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V_{ESD}	±15 ±8	KV
Junction and Storage Temperature Range	T_J, T_{STG}	-55 ~ 150	℃

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Electrical Characteristics

Parameter		Symbol	Min	Max	Units
Reverse Stand-Off Voltage		V_{RWM}	-	5	V
Reverse Breakdown Voltage	I_R = 1mA	$V_{(BR)}$	6	-	V
Reverse Leakage Current	V_R = 5V	I_R	-	1	μA
Clamping Voltage	I_{PP} = 1A	V_C	-	9.8	V
	I_{PP} = 2A		-	25	
Junction Capacitance		C_J	1.2 (Typ.)		pF

Rating and Characteristic Curves

Fig 1 Non-Repetitive Peak Pulse Power vs. Pulse Time

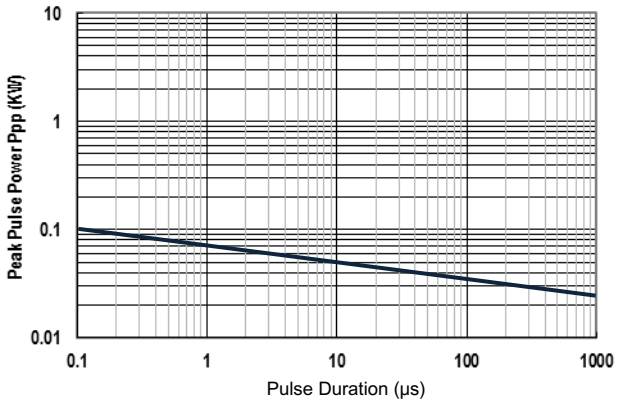


Fig 2 Clamping Voltage vs. Peak Pulse Current

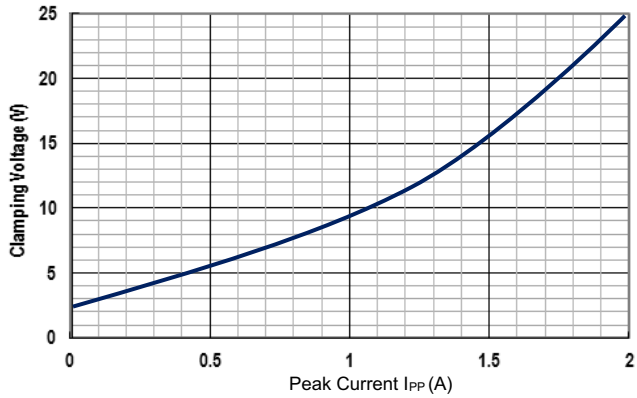


Fig 3 Admissible Power Dissipation Curve

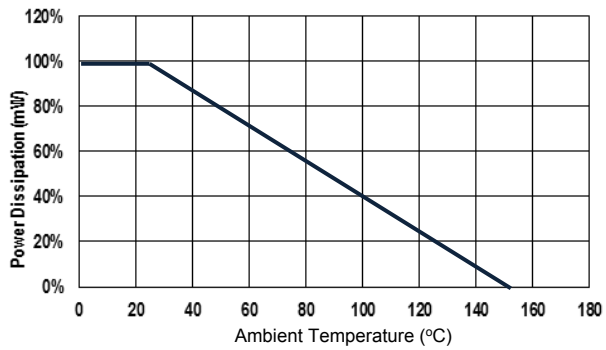


Fig 4 Typical Junction Capacitance

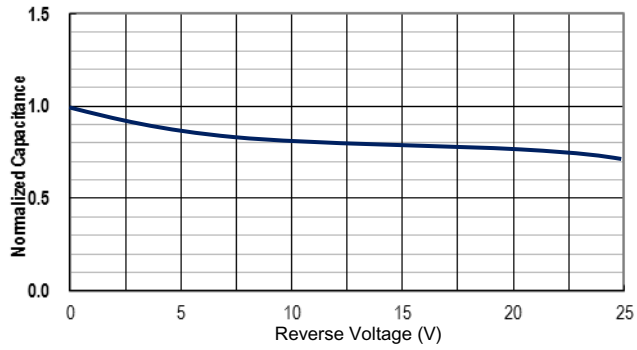
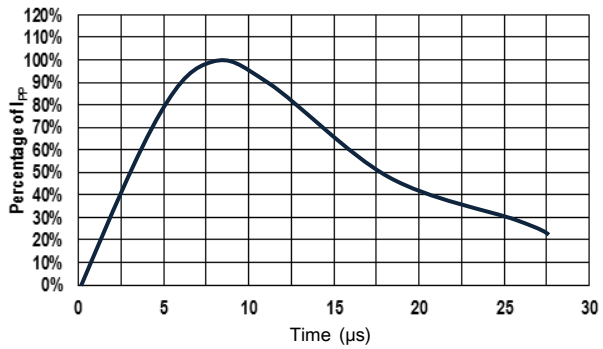


Fig 5 Pulse Waveform



Low Capacitance ESD Protection Array

Application information

Designed to protect two I/O lines, operating at 5 volts.

This device is optimized for protection of 1 line operating in excess of 3GHz.

It may also be used to protect two lines operating in excess of 2.0GHz.

Protect sensitive electronics from damage or latch-up due to ESD

During transient conditions, the steering diodes direct the transient to either the positive side of the power supply line or to ground

The internal TVS diode prevents over-voltage on the power line, protecting any downstream components

Circuit Board Layout Recommendations

Place the ESD Protection Diode near the input terminals or connectors to restrict transient coupling.

Minimize the path length between the Protection Diode and the protected line

Minimize all conductive loops including power and ground loops

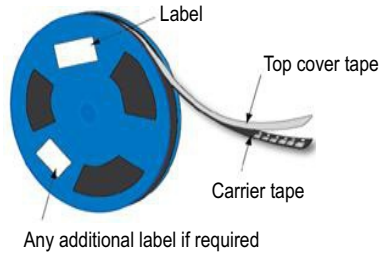
The ESD transient return path to ground should be kept as short as possible

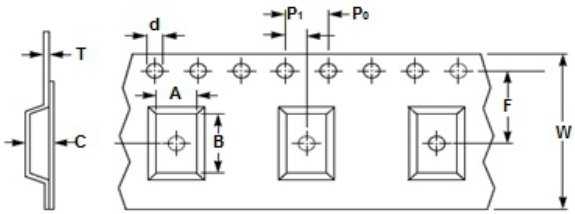
Never run critical signals near board edges

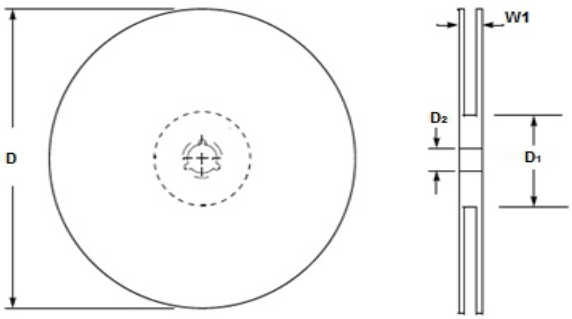
Use ground planes whenever possible

Good circuit board layout is critical for the suppression of ESD induced transients

Tape & Reel specification







Item	Symbol	Dimension (mm)
Carrier width	A	1.70 ± 0.10
Carrier length	B	1.85 ± 0.10
Carrier depth	C	0.90 ±0.10
Sprocket hole	d	1.5 ± 0.1
Reel outside diameter	D	178 ± 1
Reel inner diameter	D1	55 Min
Feed hole width	D2	13.0 ± 0.20
Sprocke hole position	E	1.75 ±0.10
Punch hole position	F	3.50 ±0.05
Punch hole pitch	P	4.00 ±0.10
Sprocke hole pitch	P0	4.00 ±0.10
Embossment center	P1	2.00 ±0.05
Overall tape thickness	T	0.23 ± 0.05
Tape width	W	8.00 ±0.20
Reel width	W1	14.4 Max