



5-Line ESD Protection Array

DESCRIPTION

- ◆ The ESDH65V0U are designed by TVS array that is to protect sensitive electronics from damage or latch-up due to ESD.
- ◆ They are designed for use in applications where board space is at a premium.
- ◆ ESDH65V0U will protect up to five lines, and may be used on lines where the signal polarities swing above and below ground.
- ◆ ESDH65V0U offer desirable characteristics for board level protection including fast response time, low operating and clamping voltage, and no device degradation.
- ◆ ESDH65V0U may be used to meet the immunity requirements of IEC 61000-4-2, level 4.
- ◆ The small SOT-563 package makes them ideal for use in portable electronics such as cell phones, PDA's, notebook computers, and digital cameras.

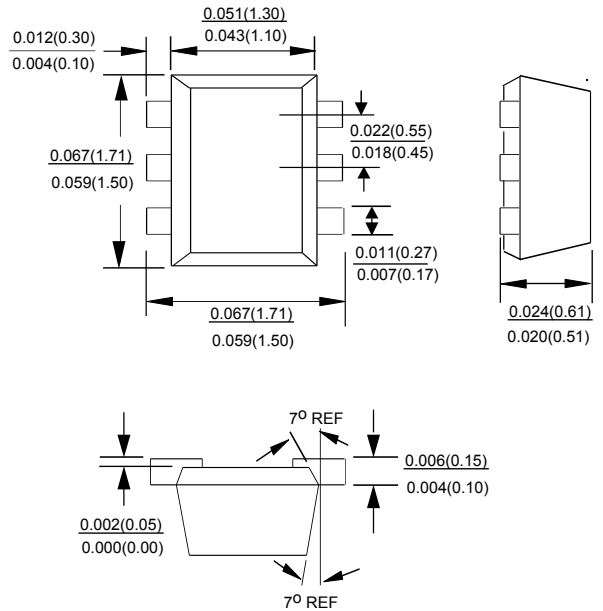
FEATURE

- ◆ Transient protection for data lines to IEC 61000-4-2 (ESD) ±15kV (air), ±8kV (contact) IEC 61000-4-4 (EFT) 40A (5/50ns)
- ◆ Protects five I/O lines
- ◆ Working voltage : 5V
- ◆ Low leakage current
- ◆ Low operating and clamping voltages

APPLICATIONS

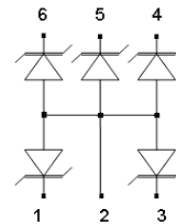
- ◆ Cellular Handsets and Accessories
- ◆ Cordless Phone
- ◆ PDA
- ◆ Notebooks and Handhelds
- ◆ Portable Instrumentation
- ◆ Digital Cameras
- ◆ MP3 Player

SOT-563 PACKAGE OUTLINE

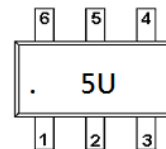


Unit : Inch (mm)

PIN CONFIGURATION (SOT-563 / SC-89)



PART MARKING





5-Line ESD Protection Array

ABSOLUTE MAXIMUM RATINGS

($T_A = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Typical	Unit
Peak Pulse Power ($t_p = 8/20 \mu\text{s}$)	Ppk	100	W
Maximum Peak Pulse Current ($t_p = 8/20 \mu\text{s}$)	Ipp	8	A
ESD per IEC 61000 – 4 – 2 (Air)	Vpp	± 15	KV
ESD per IEC 61000 – 4 – 2 (Contact)	Vpp	± 8	KV
Operating Junction Temperature	T_J	-55 ~ 125	$^\circ\text{C}$
Storage Temperature Range	T_{STG}	-55 ~ 150	$^\circ\text{C}$
Lead Soldering Temperature	T_L	260 (10sec)	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS

($T_A = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Reverse Stand – Off Voltage	V_{RWM}				5	V
Reverse Breakdown Voltage	V_{BR}	$I_t = 1\text{mA}$	6		7.6	V
Reverse Leakage Current	I_R	$V_{\text{RWM}} = 5\text{V}$, $T = 25^\circ\text{C}$			1	μA
Forward Voltage	V_F	$I_F = 10\text{mA}$			1.0	V
Clamping Voltage	V_C	$I_{\text{pp}} = 8\text{A}$, $t_p = 8/20 \mu\text{s}$			13	V
Junction Capacitance	C_J	Between I/O Pin and GND $V_R = 0\text{V}$, $f = 1\text{MHz}$			60	pF

ORDERING INFORMATION

Part Number	Package	Packing	Part Marking
ESDH65V0U	SOT-563	3K/7" Reel	5U



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TYPICAL CHARACTERISTICS

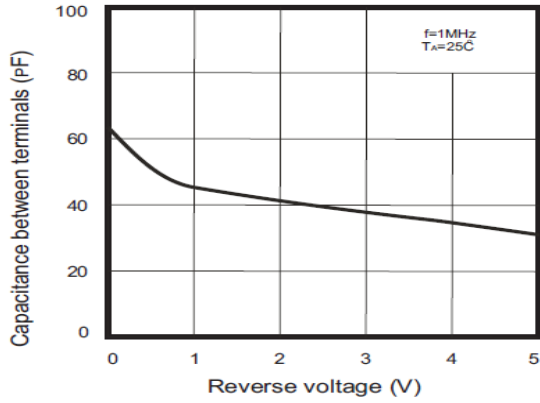


Fig 1 : Junction Capacitance V.S Reverse Voltage Applied

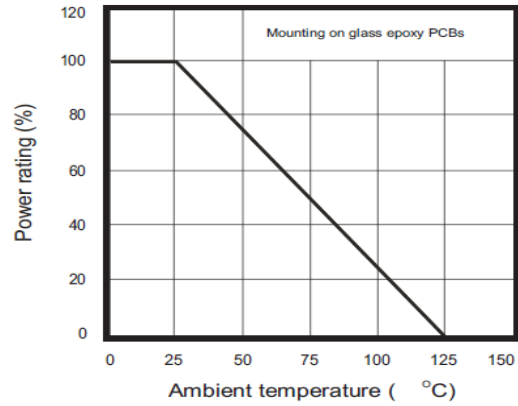


Fig 2 : Peak Plus Power V.S Exponential Plus Duration

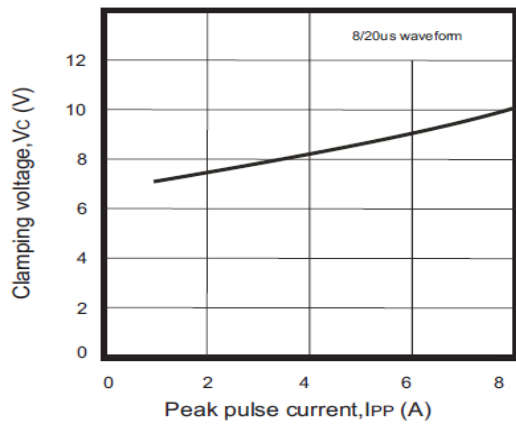
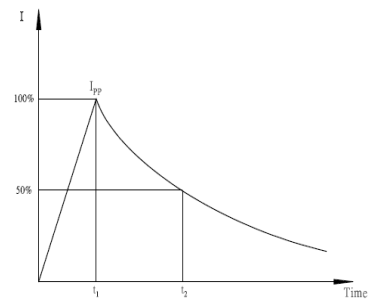


Fig 3 : Clamping Voltage VS Peak Pulse Current



t₁ = 上升时段
 t = Pulse Width (波寬)
 t₂ ~ t = 下降时段
 I_{pp} = Peak Value (峰值電流)

$10/1000 \mu s = t_1 / t_2$

Fig 4 : Forward Voltage Drop V.S Peak Forward Current



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APPLICATION NOTE

Device Connection for Protection of Five Data Lines

ESDH65V0U is designed to protect up to five data lines

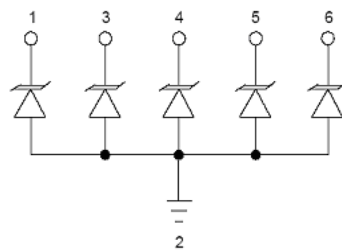
The device is connected as follows :

The TVS protection of five I/O lines is achieved by connecting pins 1, 3, 4, 5, and 6 to the data lines.

Pin 2 is connected to ground.

The ground connection should be made directly to the ground plane for best results.

The path length is kept as short as possible to reduce the effects of parasitic inductance.



Circuit Board Layout Recommendations for Suppression of ESD

Good circuit board layout is critical for the suppression of ESD induced transients. The following guidelines are recommended:

1. Place the TVS near the input terminals or connectors to restrict transient coupling.
2. Minimize the path length between the TVS and the protected line.
3. Minimize all conductive loops including power and ground loops.
4. The ESD transient return path to ground should be kept as short as possible.
5. Never run critical signals near board edges.
6. Use ground planes whenever possible.

